ETSIT
Escuela Técnica Superior de
Ingenieros de Telecomunicación

# Courses Syllabus:

| Digital Electronics (DE) | | | |
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| Code number: | 48072 | Number of ECTS: | 6 ECTS |
| Semester: | Autumn | Language: | English |

**Lecturer(s) and contact:**

- Dr. Luis Alberto Marqués Cuesta (lmarques@ele.uva.es)

**Learning goals:**

At the end of the course, the student must be able to:

- Know and understand fundamental concepts related to digital electronic circuits.
- Analyze and design (synthesize) basic digital electronic circuits from logic gates, combinational and/or sequential modules.
- Choose, among the different types of mass storage systems, those that fit a specific application.
- Use CAD tools based on hardware description languages for the design of digital blocks and the subsequent verification of their correct operation.
- Organize, plan and manage laboratory time.
- Communicate, both in writing and orally, the procedure used in the laboratory and the difficulties that may arise.

**Contents:**

UNIT 1 – FUNDAMENTALS
- 1.1.- Introduction.
- 1.2.- Boolean Algebra.
- 1.3.- Two-variable logic functions. Functional completeness.
- 1.4.- Information coding.
- 1.5.- Minimization of logic functions. Canonical form.

UNIT 2 – COMBINATIONAL CIRCUITS
- 2.1.- Introduction.
- 2.2.- AND-OR design and analysis.
- 2.3.- NAND-NOR design and analysis.
- 2.4.- Hazards.
- Lab session 1 – Structural design (1st part).

UNIT 3 – COMBINATIONAL MODULES
- 3.1.- Introduction.
- 3.2.- Decoder.
- 3.3.- Encoder.
- 3.4.- Code converter.
- 3.5.- Multiplexer.
- 3.6.- Demultiplexer.
- 3.7.- Comparator.
- 3.8.- Adder.
- Lab session 2 – Structural design (2nd part).
- Lab session 3 – RTL design.

UNIT 4 – LATCHES AND FLIP-FLOPS
- 4.1.- Introduction.
- 4.2.- Static latches.
- 4.3.- Dynamic latches.

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| 4.4.- Flip-flops.<br>UNIT 5 – SEQUENTIAL CIRCUITS<br>5.1.- Introduction.<br>5.2.- Design procedure.<br>5.3.- Moore and Mealy automata.<br>Lab session 4 – Algorithm-based description (1st part).<br>UNIT 6 – SEQUENTIAL MODULES<br>6.1.- Introduction.<br>6.2.- Storage registers.<br>6.3.- Transferring digital information. Buses.<br>6.4.- Counters.<br>6.5.- Shift registers.<br>6.6.- Operational registers.<br>Lab session 5 – Algorithm-based description (2nd part).<br>UNIT 7 – MEMORIES<br>7.1.- Introduction.<br>7.2.- Random access memories.<br>7.3.- Sequential memories. |
| Prerequisites:<br>None. |
| Assessment:<br>Midterm exam (units 1-3) and final exam (units 4-7) account for 60% of the grade. Another practical, laboratory exam accounts for 40% of the grade. |