

Courses Syllabus:

Digital Electronics (DE)			
Code number:	48072	Number of ECTS:	6 ECTS
Semester:	Autumn	Language:	English
Lecturer(s) and contact:			
<ul style="list-style-type: none"> Dr. Luis Alberto Marqués Cuesta (lmarques@ele.uva.es) 			
Learning goals:			
At the end of the course, the student must be able to:			
<ul style="list-style-type: none"> Know and understand fundamental concepts related to digital electronic circuits. Analyze and design (synthesize) basic digital electronic circuits from logic gates, combinational and/or sequential modules. Choose, among the different types of mass storage systems, those that fit a specific application. Use CAD tools based on hardware description languages for the design of digital blocks and the subsequent verification of their correct operation. Organize, plan and manage laboratory time. Communicate, both in writing and orally, the procedure used in the laboratory and the difficulties that may arise. 			
Contents:			
UNIT 1 – FUNDAMENTALS			
1.1.- Introduction.			
1.2.- Boolean Algebra.			
1.3.- Two-variable logic functions. Functional completeness.			
1.4.- Information coding.			
1.5.- Minimization of logic functions. Canonical form.			
UNIT 2 – COMBINATIONAL CIRCUITS			
2.1.- Introduction.			
2.2.- AND-OR design and analysis.			
2.3.- NAND-NOR design and analysis.			
2.4.- Hazards.			
<u>Lab session 1</u> – Structural design (1st part).			
UNIT 3 – COMBINATIONAL MODULES			
3.1.- Introduction.			
3.2.- Decoder.			
3.3.- Encoder.			
3.4.- Code converter.			
3.5.- Multiplexer.			
3.6.- Demultiplexer.			
3.7.- Comparator.			
3.8.- Adder.			
3.9.- Arithmetic-Logic Unit (ALU).			
<u>Lab session 2</u> – Structural design (2nd part).			
<u>Lab session 3</u> – RTL design.			
UNIT 4 – LATCHES AND FLIP-FLOPS			
4.1.- Introduction.			
4.2.- Static latches.			

4.3.- Dynamic latches.

4.4.- Flip-flops.

UNIT 5 – SEQUENTIAL CIRCUITS

5.1.- Introduction.

5.2.- Design procedure.

5.3.- Moore and Mealy automata.

Lab session 4 – Algorithm-based description (1st part).

UNIT 6 – SEQUENTIAL MODULES

6.1.- Introduction.

6.2.- Storage registers.

6.3.- Transferring digital information. Buses.

6.4.- Counters.

6.5.- Shift registers.

6.6.- Operational registers.

Lab session 5 – Algorithm-based description (2nd part).

UNIT 7 – MEMORIES

7.1.- Introduction.

7.2.- Random access memories.

7.3.- Sequential memories.

Prerequisites:

None.

Assessment:

Midterm exam (units 1-3) and final exam (units 4-7) account for 60% of the grade. Another practical, laboratory exam accounts for 40% of the grade.