

Courses Syllabus:

Digital Electronics (DE)			
Code number:	45012	Number of ECTS:	6 ECTS
Semester:	Autumn	Language:	English
Lecturer(s) and contact:			
<ul style="list-style-type: none"> • Dr. Luis Alberto Marqués Cuesta (lmarques@ele.uva.es) 			
Learning goals:			
At the end of the course, the student must be able to:			
<ul style="list-style-type: none"> • Know and understand fundamental concepts related to digital electronic circuits. • Analyze and design (synthesize) basic digital electronic circuits at the logic gate level. • Understand the differences between logic families and their evolution to the present. • Choose, among the different types of mass storage systems, those that fit a specific application. • Use component specification sheets to extract the most relevant data and be able to compare between different alternatives. • Work in groups to construct digital circuits from basic integrated components, and to use electronic instruments to check and test them. • Organize, plan and manage laboratory time. • Communicate, both in writing and orally, the procedure used in the laboratory and the difficulties that may arise. 			
Contents:			
UNIT 1 – FUNDAMENTALS			
1.1.- Introduction.			
1.2.- Boolean Algebra.			
1.3.- Two-variable logic functions. Functional completeness.			
1.4.- Information coding.			
1.5.- Minimization of logic functions. Canonical form.			
UNIT 2 – LOGIC FAMILIES			
2.1.- Introduction.			
2.2.- Electrical parameters.			
2.3.- The MOS transistor.			
2.4.- The CMOS family.			
2.5.- Other families. Comparative.			
UNIT 3 – COMBINATIONAL CIRCUITS			
3.1.- Introduction.			
3.2.- AND-OR design and analysis.			
3.3.- NAND-NOR design and analysis.			
3.4.- Hazards.			
Lab session 1 – Implementation of a combinational circuit with logic gates.			
UNIT 4 – COMBINATIONAL MODULES			
4.1.- Introduction.			
4.2.- Decoder.			
4.3.- Encoder.			
4.4.- Code converter.			
4.5.- Multiplexer.			
4.6.- Demultiplexer.			

4.7.- Comparator.

4.8.- Adder.

Lab session 2 – Circuit implementation using combinational modules.

UNIT 5 – LATCHES AND FLIP-FLOPS

5.1.- Introduction.

5.2.- Static latches. D-type latch.

5.3.- RS latch. Dynamic latches.

5.4.- D-type flip-flop.

5.5.- JK and T-type flip-flops.

UNIT 6 – SEQUENTIAL CIRCUITS

6.1.- Introduction.

6.2.- Design procedure.

6.3.- Moore and Mealy automata.

Lab session 3 – Implementation of a sequential circuit.

UNIT 7 – SEQUENTIAL MODULES

7.1.- Introduction.

7.2.- Storage registers.

7.3.- Transferring digital information. Buses.

7.4.- Counters.

7.5.- Shift registers.

7.6.- Operational registers.

Lab session 4 – Implementation of a register.

UNIT 8 – MEMORIES

8.1.- Introduction.

8.2.- Random access memories.

8.3.- Sequential memories.

Lab session 5 – Final lab exam.

Prerequisites:

None.